

FIG. 1A

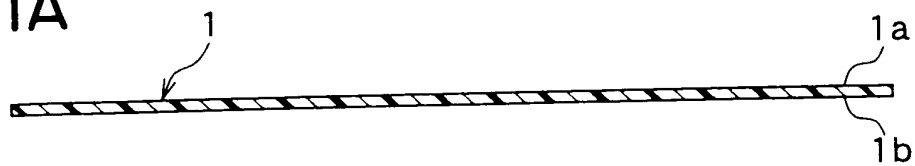


FIG. 1B

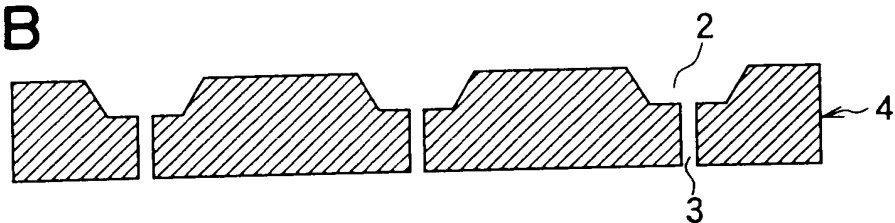


FIG. 1C

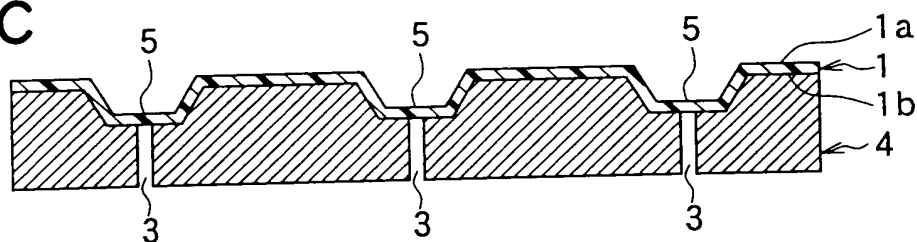


FIG. 1D

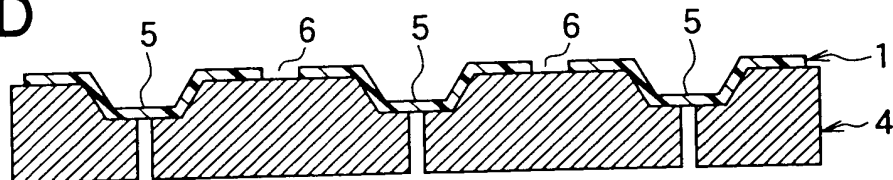


FIG. 1E

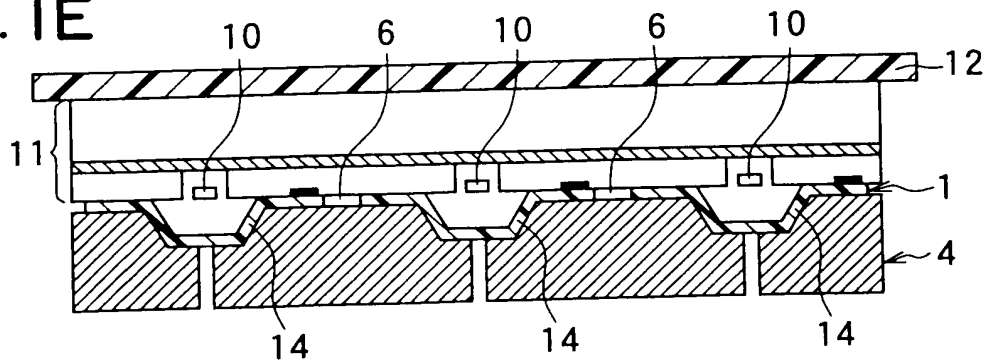


FIG. 2A

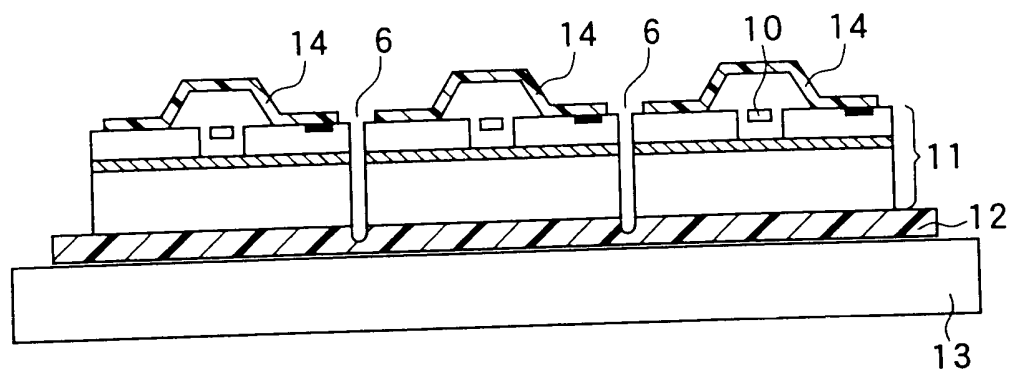


FIG. 2B

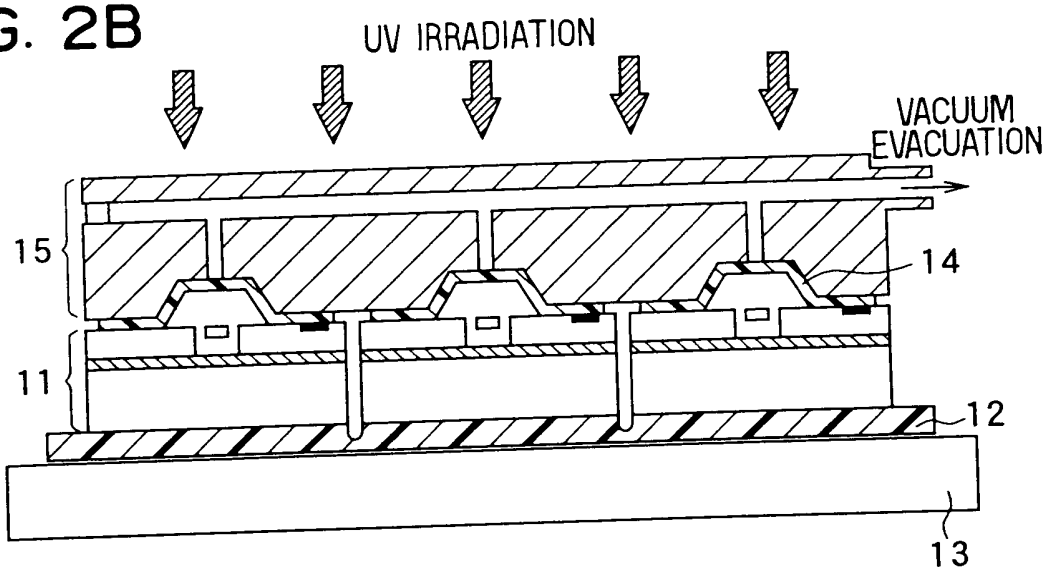


FIG. 2C

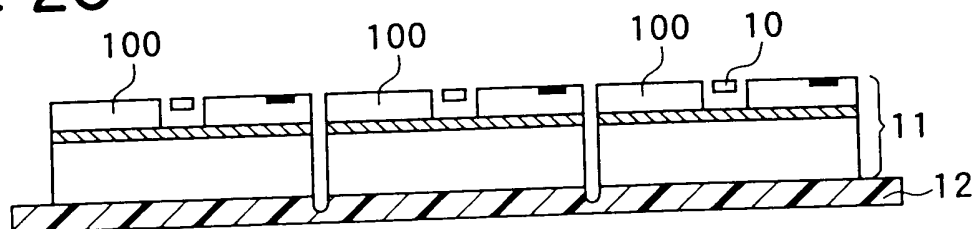


FIG. 3A

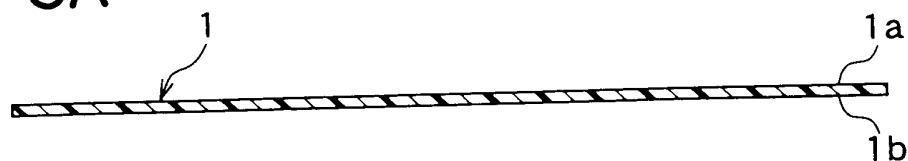


FIG. 3B

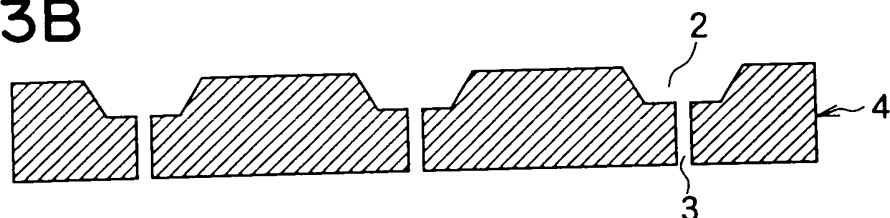


FIG. 3C

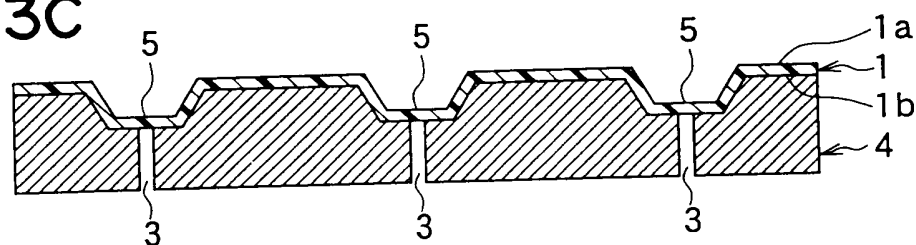


FIG. 3D

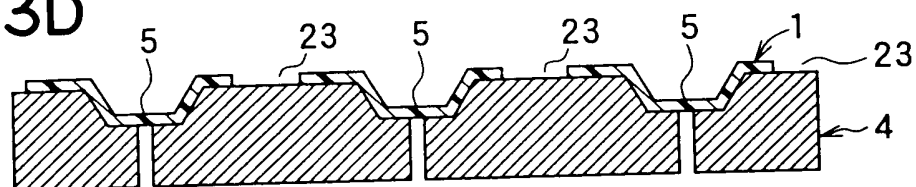


FIG. 3E

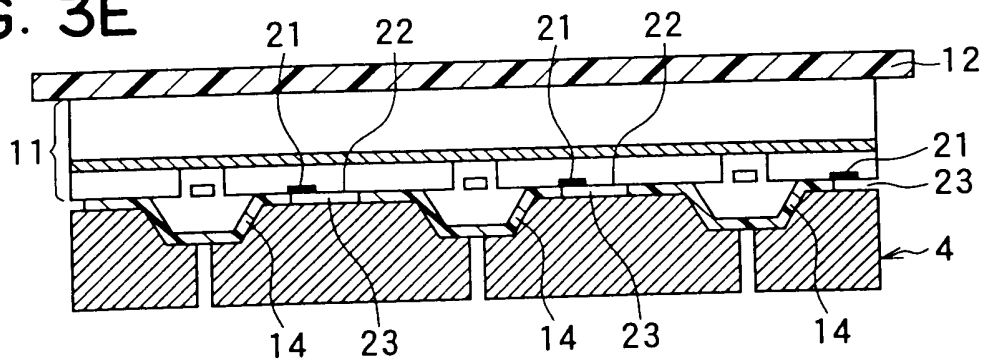


Figure 1 is a cross-sectional view of a semiconductor device. It shows three identical units on a substrate 12. Each unit has a base layer 11, a central block 200, and a top structure with layers 14, 21, and 23. The units are separated by vertical dividers.

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 30 with a base layer 32, a dielectric layer 31, and a conductive layer 33. A central structure 10 is formed on the dielectric layer, with a conductive pad 21 and a conductive line 23. A conductive line 14 is also shown. A conductive layer 34 is formed on the right side of the substrate.

FIG. 6

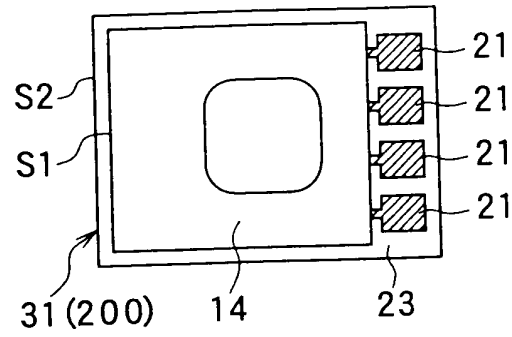


FIG. 7A

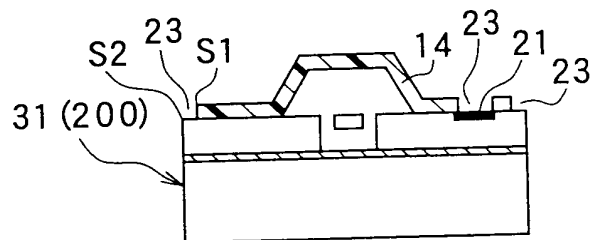


FIG. 7B

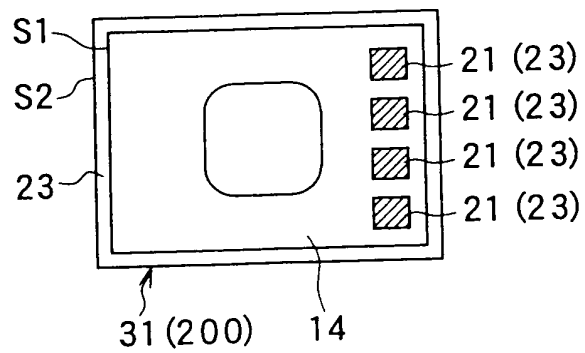


FIG. 8A

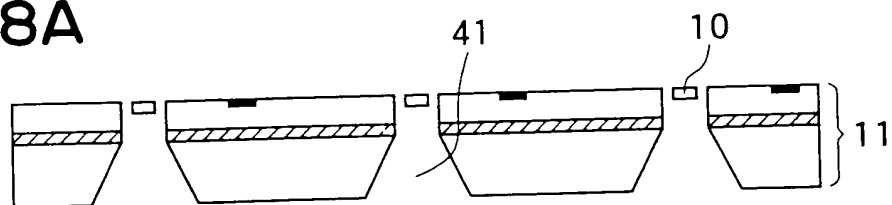


FIG. 8B

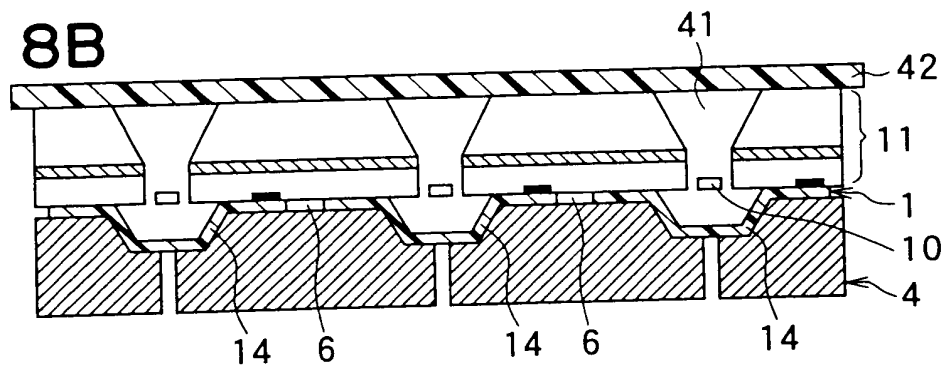


FIG. 8C

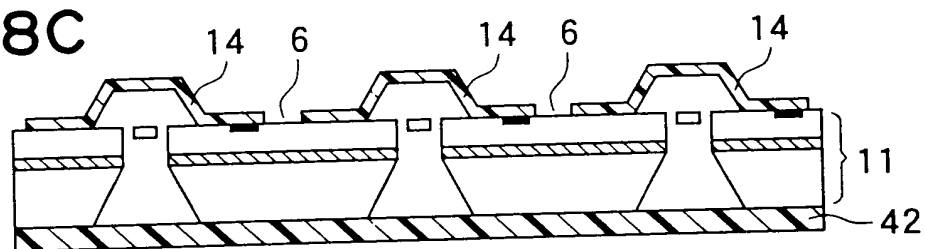


FIG. 8D

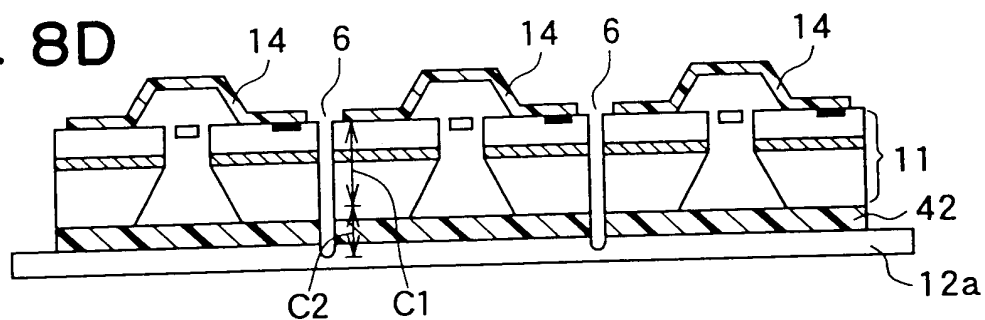


FIG. 8E

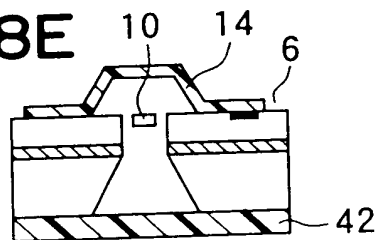


FIG. 8F

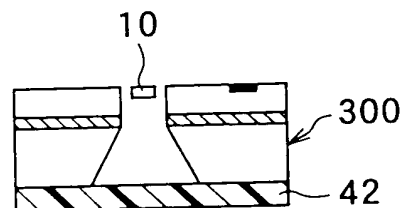


FIG. 9

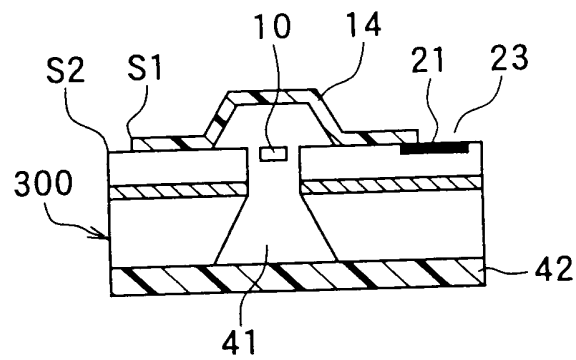


FIG. 10

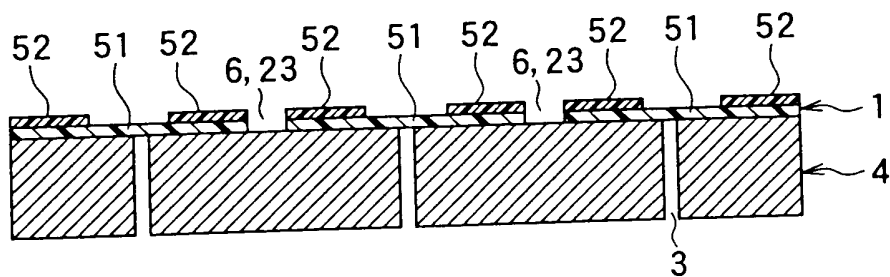


FIG. 11A

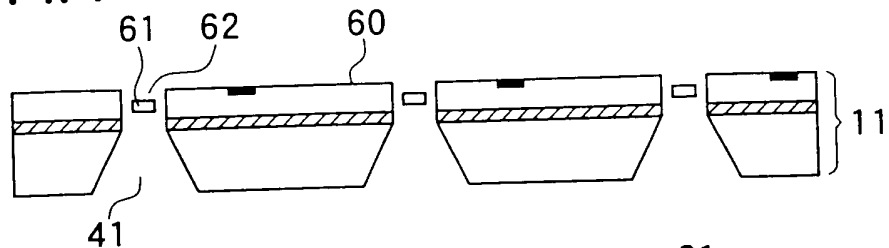


FIG. 11B

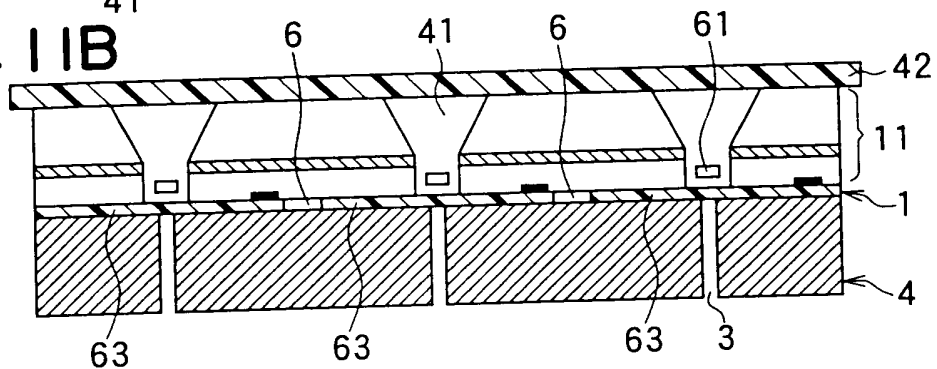


FIG. 11C

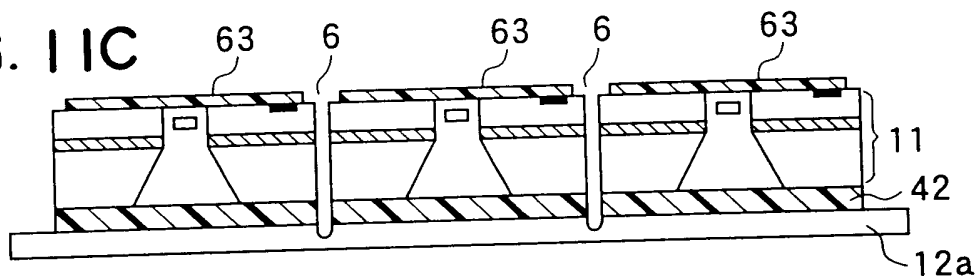


FIG. 11D

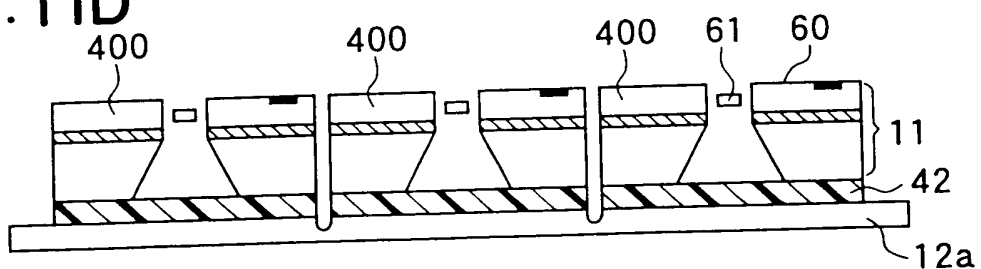


FIG. 11E

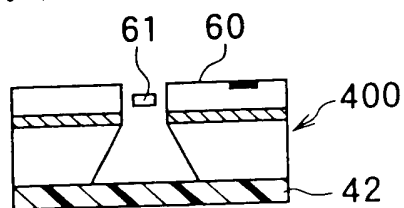


FIG. 12

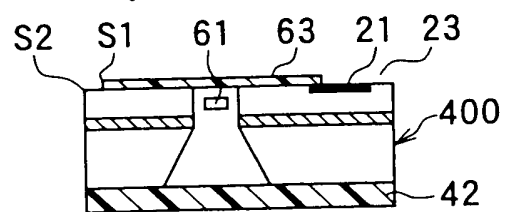


FIG. 14A

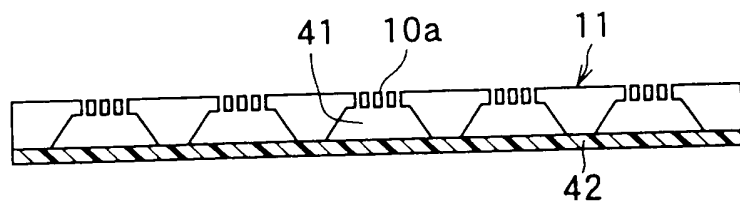


FIG. 14B

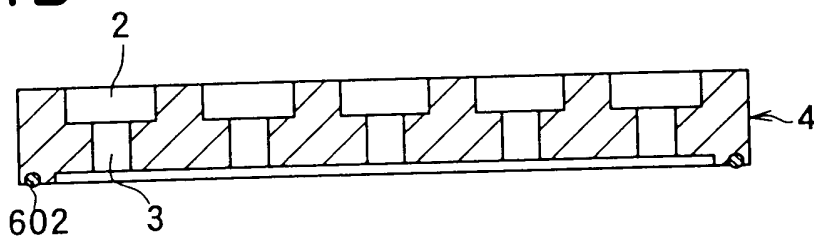


FIG. 14C

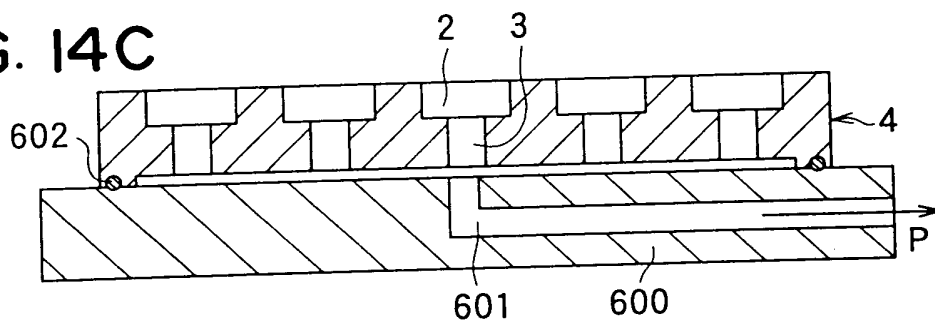


FIG. 14D

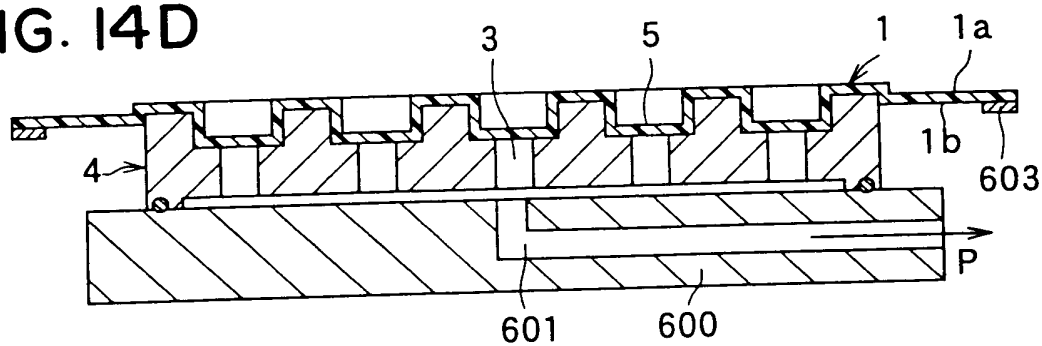


FIG. 15A

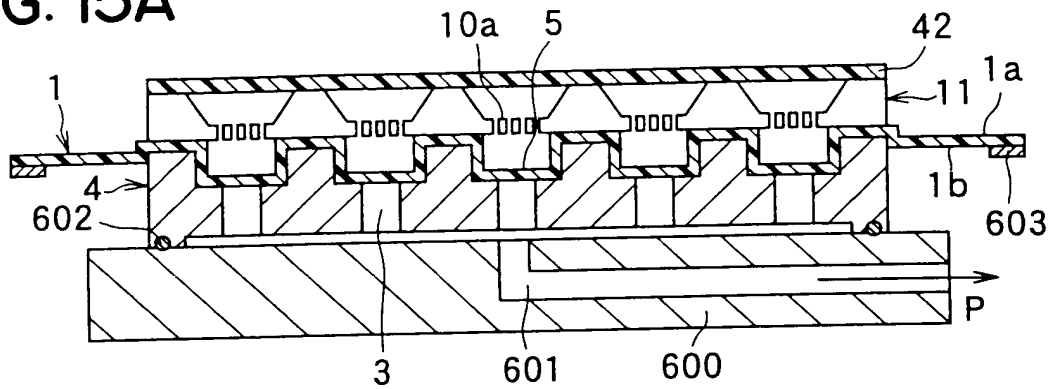


FIG. 15B

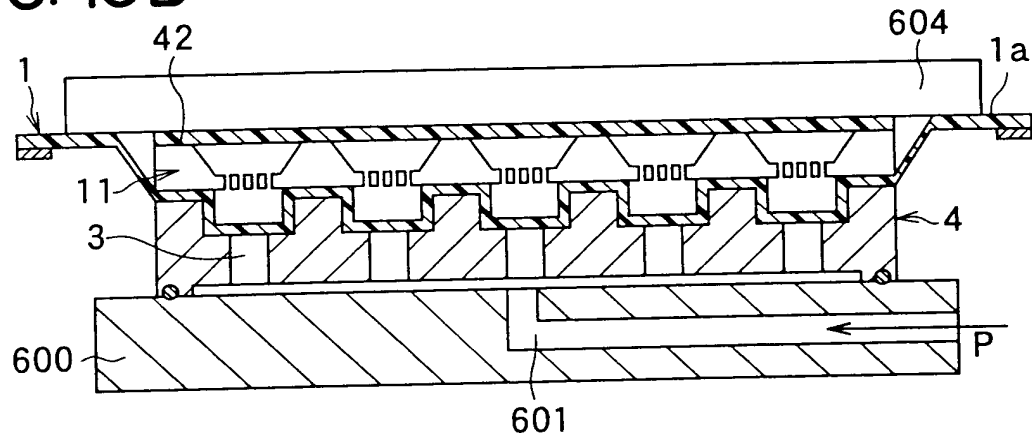


FIG. 15C

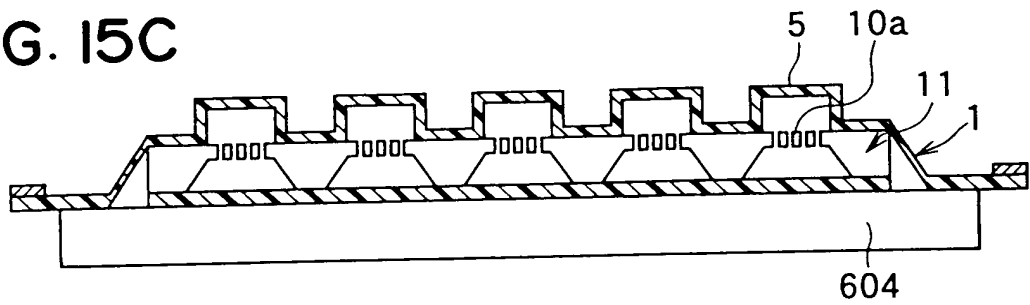


FIG. 16A

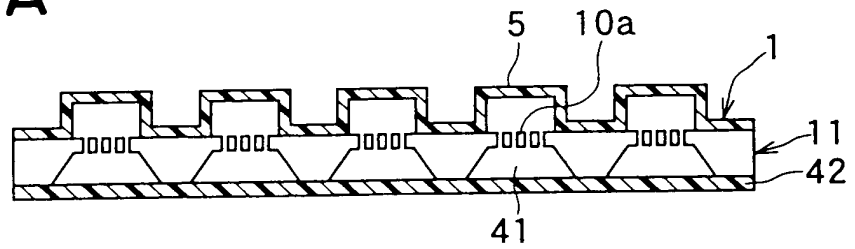


FIG. 16B

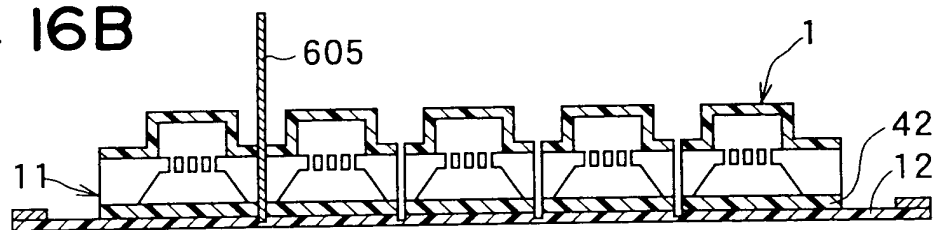


FIG. 16C

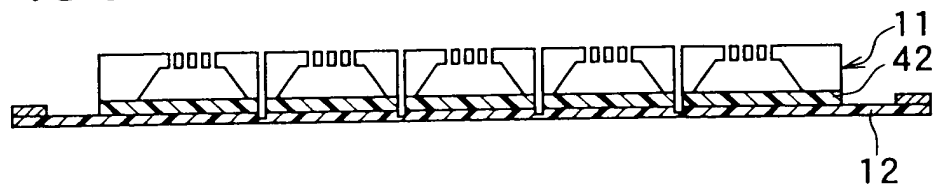


FIG. 17A

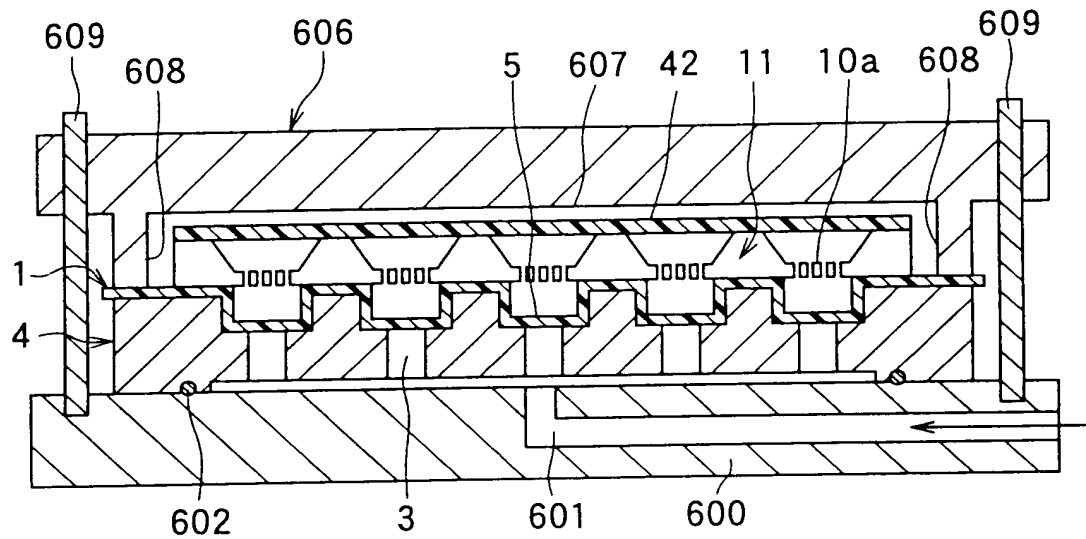


FIG. 17B

